

SYSTEM AND METHOD FOR ENCODING CONSTANT  
OPERANDS IN A WIDE ISSUE PROCESSOR

ABSTRACT OF THE DISCLOSURE

For use in a data processor comprising an instruction  
5 execution pipeline comprising N processing stages, a system and  
method of encoding constant operands is disclosed. The system  
comprises a constant generator unit that is capable of  
generating both short constant operands and long constant  
operands. The constant generator unit extracts the bits of a  
10 short constant operand from an instruction syllable and right  
justifies the bits in an output syllable. For long constant  
operands, the constant generator unit extracts K low order bits  
from an instruction syllable and T high order bits from an  
extension syllable. The right justified K low order bits and  
15 the T high order bits are combined to represent the long  
constant operand in one output syllable. In response to the  
status of op code bits located within a constant generation  
instruction, the constant generator unit enables and disables  
multiplexers to automatically generate the appropriate short or  
20 long constant operand.